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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,477	01/28/2004	Leonard Forbes	M4065.0381/P381-A	9433
24998	7590	06/16/2005	EXAMINER	
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP			THOMAS, TONIAE M	
2101 L Street, NW			ART UNIT	
Washington, DC 20037			PAPER NUMBER	
			2822	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/765,477

Applicant(s)

FORBES ET AL.

Examiner

Toniae M. Thomas

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 68-91 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 68-91 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 01/28/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/765,477, which is a divisional of Application Serial No. 09/808,114 filed on 15 March 2001, now US Patent No. 6,734,510.
2. The preliminary amendment filed on 28 January 2004 cancelled claims 1-67. Accordingly, claims 68-91 are currently pending.
3. The information disclosure statement filed 28 January 2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. Accordingly, the non-patent literature documents corresponding to citation letters I, J, K have not been considered. While these documents were cited in the parent application, Serial No. 09/808,114, the documents are not available in the Image File Wrapper (IFW) database and, therefore, cannot be considered by the examiner.
4. In response to this Office action, Applicant is required to submit a copy of each of the aforementioned foreign patent and non-patent literature documents for examiner's review.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

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5. Claims 68-89 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claim language *said first conductive layer* lacks antecedent basis (claim 68, line 4).

Antecedent basis for the claim language *said P+ type conductive layer* is unclear (claim 89, line 11). The claim language as recited in claim 89 does not clearly indicate to which of the at least two substantially vertical P+ type conductive layer regions the phrase *said P+ type conductive layer* is referring.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 68, 69, 90, and 91 are rejected under 35 U.S.C. 102(e) as being anticipated by Mandelman et al. (US 6,097,070).¹

Regarding claims 68 and 69

The Mandelman et al. patent (Mandelman) discloses a method of forming a semiconductor transistor (figs. 2, 3A-3C and accompanying text). The method comprises: forming a first gate dielectric 27 over a substrate 20 (fig. 3A; col. 3, line 59; and col. 4, lines 10-11); forming a first type conductive gate region 25 over the first gate dielectric (fig. 3B and col. 4, lines 12-15);² forming a dielectric layer 29 on the sides of the first type conductive layer (fig. 3C and col. 4, lines 19-29); forming a second gate dielectric 28 over the substrate (fig. 3C and col. 4, lines 19-29); forming a second type conductive gate region 26 over the second gate dielectric, adjacent to the dielectric layer, and on the sides of the first type conductive region (fig. 3C and col. 4, lines 35-39); and forming source and drain regions 21 in the substrate to define a channel region between them and beneath the first and second conductive type gate regions (fig. 2 ad col. 5, lines 1-5).

In one preferred embodiment, the first type conductive region is of P+ conductivity type and the second type conductive region is of N+ conductivity type (col. 4, lines 12-15 and col. 4, lines 36-50).

¹ The Applicant submitted the Mandelman et al. patent as prior art (see PTO Form 1449 filed on 28 January 2004). The patent reference was also cited in the parent application, Serial No. 09/808,114.

Regarding claims 90 and 91

Again, Mandelman discloses a method of forming a semiconductor transistor (figs. 2, 3A-3C and accompanying text). The method comprises: providing a substrate 20 (fig. 3A and col. 3, line 59); forming a first gate dielectric layer 27 over the substrate (fig. 3A and col. 4, lines 10-11); forming a first gate electrode 25 having sidewalls over the first gate dielectric layer (fig. 3B and col. 4, lines 12-15, wherein in one preferred embodiment the first gate electrode has a first work function (abstract, lines 11-13 and col. 4, lines 36-50); forming a dielectric layer 29 on the sidewalls of the first gate electrode (fig. 3C and col. 4, lines 19-29); forming a second gate dielectric 28 over the substrate (fig. 3C and col. 4, lines 19-29); forming a pair of second gate electrodes 26 over the second gate dielectric and adjacent to the dielectric layer, the second gate electrodes being separated from the first gate electrode by the dielectric layer (fig. 3C and col. 4, lines 35-39), wherein in one preferred embodiment the pair of second gate electrodes has a second work function which is different than the first work function (abstract, lines 11-13 and col. 4, lines 36-50); forming a conductive cap 23 over each of the gate electrodes (fig. 3C and col. 4, lines 54-56); and forming insulating sidewalls 22 adjacent to the conductive cap and the gate electrodes (fig. 2 and col. 4, line 66 - col. 5, line 1).

² In one preferred embodiment, the gate region 25 is a P+ type conductive gate (col. 4, lines 12-15). In this Office action, the P+ conductive type is designated as the first conductive type.

In one preferred embodiment, the second work function is more negative than the first work function (col. 4, lines 36-50).

Allowable Subject Matter

7. Claims 70-88 would be allowable if rewritten to overcome the rejection under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The prior art of record does not anticipate, teach or suggest a method of forming a semiconductor transistor substantially as claimed, wherein the method comprises forming the P+ type conductivity region as recited in claim 70.

8. Claim 89 would be allowable if rewritten or amended to overcome the rejection under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action. Mandelman does anticipate teach or suggest the following limitations recited in claim 89: selectively etching the P+ type conductive layer to leave at least two substantially vertical P+ type conductive layer regions over the first gate dielectric; removing a portion of the first gate dielectric by selectively etching to the substrate, thereby leaving the vertical P+ type conductive layer regions over the remaining first gate dielectric; and etching the N+ type conductive layer to leave at least two structures, the two structures including the vertical P+ type conductive layer regions and the

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adjacent regions of the N+ type conductive layer. There is no teaching or suggestion within the prior art of record to modify Mandelman according to the claimed invention. Furthermore, while Mandelman discloses forming a dielectric layer 29 on the sidewalls of the P+ type conductive region 25, Mandelman does not anticipate, teach or suggest forming the dielectric layer of a nitride layer. There is no teaching or suggestion within the prior art of record to modify Mandelman by forming the dielectric layer of a nitride layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
08 June 2005



Mary Wilczewski
Primary Examiner